This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

Fin Shape Impact on FinFET Leakage With Application to Multithreshold and Ultralow-Leakage FinFET Design

Brad D. Gaynor and Soha Hassoun, *Senior Member, IEEE*

***Abstract*— FinFETs have emerged as the solution to short channel effects at the 22-nm technology node and beyond. Previously, there have been few studies on the impact of fin cross section shape on transistor leakage. We show for the first time that fin shape significantly impacts transistor leakage in bulk tri-gate nFinFETs with thin fins when the fin body doping profile is optimized to minimize leakage. We show that a triangular fin reduces leakage current by 70% over a rectangular fin with the same base fin width. We describe how fin shape can be used to implement multithreshold nFinFETs without increasing chip area consumption. We also describe how by combining triangular fins with existing gate–source/drain underlap multithreshold techniques, it is possible to design ultralow-power nFinFETs with less than 1 pA/μm leakage current while maintaining high performing I_{ON}/I_{OFF}, threshold voltage, and subthreshold swing.**

***Index Terms*— FinFET, leakage, multithreshold, semiconductor device modeling.**

I. Introduction

FinFETs have emerged as the solution to short channel effects (SCEs) at the 22-nm technology node and beyond [1]. Emerging production and research bulk tri-gate FinFET devices are rapidly increasing in complexity. State-of-the-art production devices incorporate rounded corners, work function (WF) engineering, channel strain engineering, and fin body doping [2]. In addition, research devices incorporate multithreshold voltage (V_{th}) techniques via WF engineering and gate–source/drain (G–S/D) overlap [3] and fin doping [4], [5].

Low leakage devices are a key enabler for long-life System-on-Chip applications with ultralow-power standby requirements. While bulk FinFETs show improved leakage performance over planar CMOS, leakage persists due to SCEs and gate-induced drain leakage (GIDL) [6]. Leakage due to SCEs decreases as fin widths decreases [7]; however, etching thinner fins is a significant challenge [8]. GIDL, caused by band-to-band tunneling (BTBT), where the drain region extends under the gate, decreases with thinner fins [9]. However, GIDL is difficult to eliminate, because GIDL current increases as the gate WF moves away from the band edges and due to the junction abruptness of the fin body doping. Reducing leakage requires sacrificing drive current; therefore, it is desirable to investigate tradeoffs between I_{ON} and I_{OFF}, and to provide chip designers control of the leakage/saturation current tradeoff via a multithreshold technology process.

Because FinFET performance is determined in large part by the fin geometry, it is intuitive that fin cross section shape will have an impact on leakage. However, previous studies of fin shape were primarily focused on evaluating the impact on SCEs, and provided only preliminary investigations on leakage. Liu *et al.* [10] reported that leakage increased in silicon on insulator FinFETs as the fin cross-sectional shape changes from rectangular to triangular to trapezoidal. In their study, the width of the fin base changed from 13 (rectangular) to 92 (triangular) to 140 nm (trapezoidal). We believe that the increase in leakage is due to the increase in fin width, not the change in cross-sectional shape. Recently, Wu *et al.* [11] reported that fin shape has a negligible impact on leakage performance. However, this result is neither conclusive nor generalizable as it is specific to a particular fin body doping.

Prior multithreshold FinFET research has focused on SOI (not bulk) FinFET technologies. Proposed multithreshold techniques for SOI FinFETs include WF engineering, G–S/D overlap, and active fin doping. WF engineering is required to produce functional tri-gate FinFETs with undoped active fins and midgap gate metal WF [12]. Tawfik and Kursun [13] proposed WF engineering as a multithreshold technique for FinFET. It is shown in Section III-B that this approach is incompatible with bulk FinFET design. Tawfik and Kursun also proposed the G–S/D overlap technique [3]. Negative G–S/D overlap (underlap) was shown effective in reducing leakage and incurs no additional manufacturing steps. Because this technique relies on extending the source and drain away from the gate, it may require increasing the transistor footprint when the underlap length is greater than the source/drain extensions or when there is insufficient source/drain extension margin to make a low-resistivity contact to metal layer 1.

We show in this paper for the first time that fin shape significantly impacts leakage in bulk tri-gate nFinFETs with thin fin widths when the fin body doping is optimized to minimize leakage. We describe how fin shape can be used to implement multithreshold nFinFETs without consuming

Manuscript received January 27, 2014; revised April 14, 2014 and May 29, 2014; accepted June 13, 2014. The review of this paper was arranged by Editor D. Esseni.

B. D. Gaynor is with the Department of Electrical and Computer Engineering, Tufts University, Medford, MA 02155 USA (e-mail: bradgaynor@alumni.tufts.edu).

S. Hassoun is with the Department of Computer Science, Tufts University, Medford, MA 02155 USA (e-mail: soha@cs.tufts.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2014.2331190

0018-9383 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

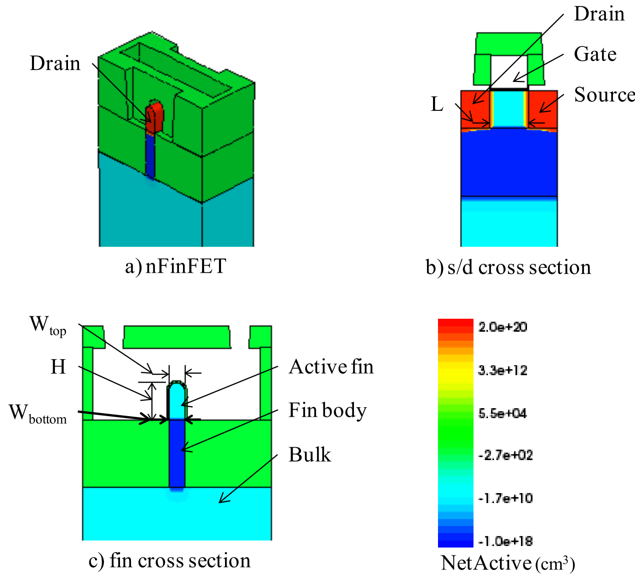

Fig. 1. Doping concentration of nFinFET structure (a) isomorphic view, (b) source/drain cross section cut at the middle of fin, and (c) fin cross section cut at the middle of channel.

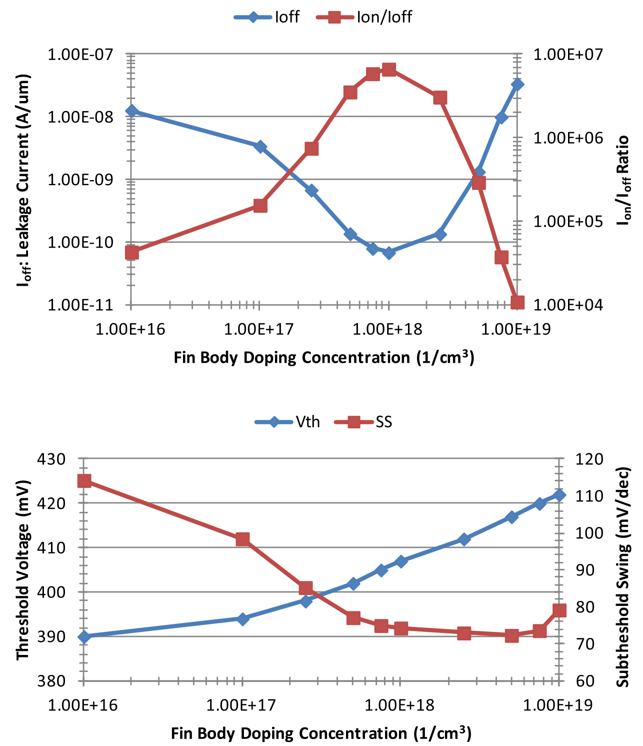

Fig. 2. I_{OFF} and I_{ON}/I_{OFF} ratio of rectangular nFinFET as a function of fin body doping (top). V_{th} and SS of rectangular nFinFET as a function of fin body doping (bottom). Active fin is undoped with concentration = 1e15.

TABLE I
nFINFET MODEL GEOMETRY PARAMETERS

Parameter	Description	Value
L	Gate length	34 nm
H	Fin height	35 nm
W_{bottom}	Width of the bottom of the active fin	15 nm
W_{top}	Width of the top of the active fin	15 nm

additional integrated circuit (IC) area. We also demonstrate the compatibility of fin shape with the existing G–S/D overlap multithreshold techniques. Our results confirm that control of fin cross-section shape provides the potential to realize multithreshold and ultralow-power FinFETs within a single process family.

II. EXPERIMENTAL METHODOLOGY

We base our analysis on the 22-nm bulk nFinFET Technology Computer Aided Design (TCAD) model (Fig. 1) adapted from [14]. This model represents the transistor features described in [2]. The key geometries shown in Table I have been selected to correspond with Intel's recent bulk FinFET production process [15]. The corner radius of the rounded fin is set to ½W_{top} to minimize corner effects. All other model parameters take the default value unless otherwise specified.

The TCAD simulations include physical models for stress effects, crystal orientation dependent quantum effects, BTBT, and drift diffusion with mobility degradation as found in [14]. The drift-diffusion models include adjusted carrier velocity saturation with the values recommended in [16]. The inversion and accumulation layer mobility model with auto-orientation accounts for the sidewall-angle dependent surface orientation of the fin, with model parameters well calibrated to experimental data [17]. The thin-layer mobility models are calibrated with parameters from [18] to capture quantum-mechanical confinement effects. The density-gradient quantum correction model with auto-orientation captures orientation-dependent quantum corrections calibrated to the solution of the Poisson–Schrödinger equations by the Sentaurus band structure [19]. The Schenk BTBT model [20] is used to simulate GIDL leakage.

Manoj *et al.* described the appropriate fin body doping required to optimize leakage in bulk FinFETs [6]. It is recommended that the active fin remain undoped to maximize carrier mobility. Leakage, however, increases under the active fin due to SCEs when there is insufficient fin body doping. There is insufficient gate control on the fin body, below the surface of the shallow trench isolation, to suppress leakage. However, excess body doping results in GIDL due to BTBT at the interface between the n^+ drain and the fin body. These competing mechanisms, SCEs and GIDL, are balanced at the optimum doping concentration of 1e18 1/cm^3. This fin body doping optimization must be performed before meaningful assessment of the impact of fin shape on leakage.

Prior to evaluating nFinFET leakage performance, the device doping is optimized as described in [6]. We sweep the p-type fin body doping concentration from 1e16–1e19 1/cm^3. The active fin is undoped with a p-type concentration of 1e15 1/cm^3. The results are shown in Fig. 2. The optimal I_{OFF} is achieved with a fin body doping concentration of 1e18 1/cm^3, consistent with prior results. I_{OFF} represents the total off state leakage current, including I_{SOFF} (SCE) and I_{XOFF} (junction leakage, GIDL). The optimal I_{ON}/I_{OFF} ratio also corresponds to a fin body doping concentration of 1e18 1/cm^3,

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

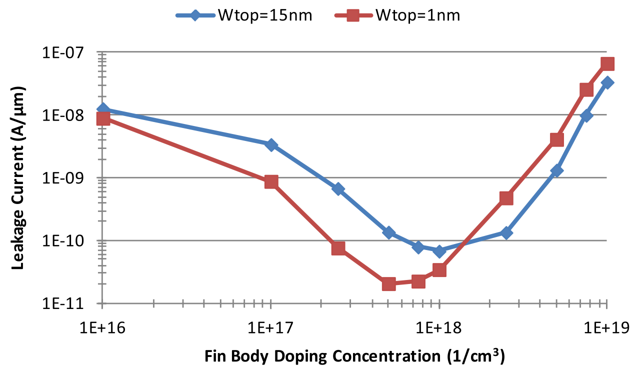

Fig. 3. I_{OFF} of rectangular and triangular nFinFET as a function of fin body doping. Active fin is undoped with concentration = 1e15.

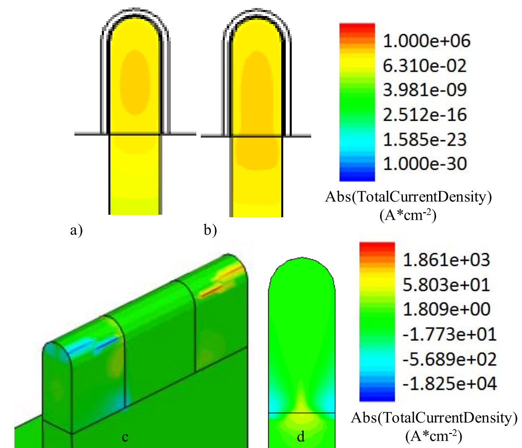

Fig. 4. I_{OFF} current density distribution of rectangular nFinFET with (a) fin body doping concentration = 1e18 1/cm^3, fin cross section cut at the middle of fin, (b) fin body doping concentration = 5e17 1/cm^3, fin cross section cut at the middle of fin, (c) current density distribution difference between the two nFinFETs, and (d) cross section of Fig. 4(c) cut at the drain/channel interface. The higher 1e18 1/cm^3 doping concentration is required to suppress leakage through the center and underneath the fin at the expense of BTBT.

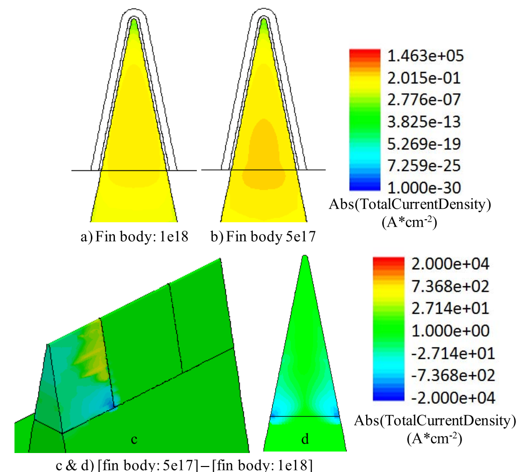

Fig. 5. I_{OFF} current density distribution of triangular nFinFET with (a) fin body doping concentration = 1e18 1/cm^3, fin cross section cut at middle of fin, (b) fin body doping concentration = 5e17 1/cm^3, fin cross section cut at the middle of fin, (c) current density distribution difference between the two nFinFETs, and (d) cross section of Fig. 5(c) cut at the drain/channel interface. While a slight increase in leakage current through the fin is observed due to increased doping, the reduction in BTBT at the base of the active fin yields an overall leakage improvement for the triangular nFinFET with fin body doping = 5e17 1/cm^3.

indicating no disproportionate saturation current degradation due to the fin body doping. V_{th} changes 32 mV over the simulated range, with a value of 407 mV at the optimum design point. V_{th} is extracted using the maximum transconductance method with V_d=0.05 V. The subthreshold swing (SS) is 74.3 mV/dec at the optimal design point. The SS is extracted at a gate voltage (V_g) of 0.3 V. The SS performance is relatively flat over the range 5e17–7.5e18 1/cm^3. Therefore, we expect doping changes within this range to have minimal impact on transistor speed.

To compare different fin shapes, we report all I_{ON} and I_{OFF} values normalized to the effective transistor width (W_{eff}), consistent with previously reported FinFET transistor performance metrics in [15]. W_{eff} is the component of the fin cross section perimeter adjacent to the gate oxide, calculated simply using the Pythagorean theorem for the fin sides and the area of the semicircle with corner radius set to $W_{\mathrm{top}}/2$ for the fin top

$$W_{\mathrm{eff}} = 2\sqrt{\left(\frac{W_{\mathrm{bottom}} - W_{\mathrm{top}}}{2}\right)^2 + \left(H - \frac{W_{\mathrm{top}}}{2}\right)^2} + \pi\frac{W_{\mathrm{top}}}{2}.$$

III. Results

A. Minimal Leakage Requires Joint Selection of Fin Shape and Fin Doping

We first examine the interaction of fin body doping and fin shape. I_{OFF} for the nFinFET with maximum $W_{\mathrm{top}} = 15$ nm (rectangular) and minimum $W_{\mathrm{top}} = 1$ nm (triangular) is plotted as a function of fin body doping (Fig. 3). The triangular nFinFET exhibits a 70% reduction in I_{OFF} over the rectangular design. The optimal fin body doping profile for the triangular nFinFET is 5e17 1/cm^3, less than the optimum doping for the rectangular nFinFET.

The I_{OFF} current density distribution for the optimal doping concentration of a rectangular FinFET (1e18 1/cm^3) is shown in Fig. 4(a). With the lower doping concentration (5e17 1/cm^3) the leakage through and below the active fin increases significantly due to SCEs (Fig. 4(b)). The change in the current density distribution of Fig. 4(b) with reference to Fig. 4(a) results in increasing leakage through the center of the fin due to SCEs and decreasing leakage due to BTBT at the fin corners of the drain-active fin interface (Fig. 4(c) and (d)). However, despite the reduction in BTBT with the lower doping profile, the total leakage current increases as the doping is changed from 1e18 1/cm^3 to 5e17 1/cm^3.

Fig. 5 shows the I_{OFF} current density distribution for a triangular fin with $W_{\mathrm{top}} = 1$ nm. As in Fig. 4, there is an increasing leakage current due to SCEs and decreasing leakage current due to BTBT with reduced doping concentration. However, the total leakage current is lower for the triangular FinFET at the reduced doping concentration relative to the rectangular FinFET. The tradeoff between the SCEs and BTBT effects is

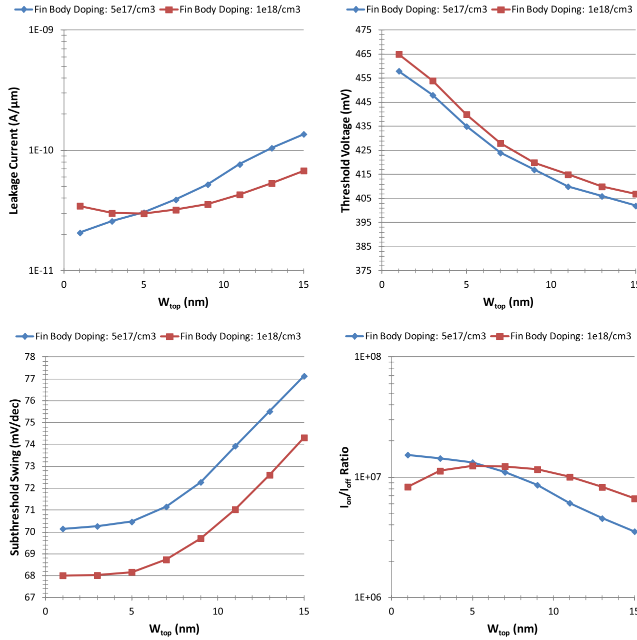

Fig. 6. Performance comparison of nFinFET as a function of fin shape: $I_{\rm OFF}$ (top left), $V_{\rm th}$ (top right), SS (bottom left), $I_{\rm ON}/I_{\rm OFF}$ ratio (bottom right).

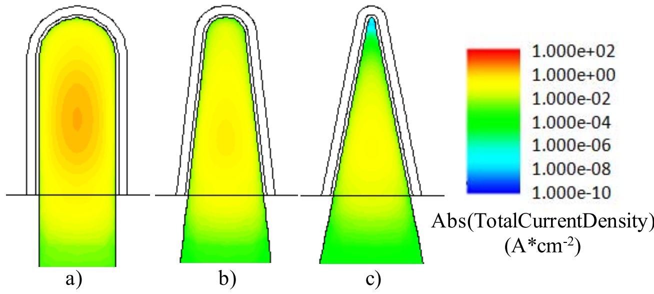

Fig. 7. $I_{\rm OFF}$ current density distribution of nFinFET with (a) rectangular fin cross section ($W_{\rm top} = 15$ nm), (b) trapezoidal fin cross section ($W_{\rm top} = 7$ nm), and (c) triangular fin cross section ($W_{\rm top} = 1$ nm), cut at the middle of channel. Rounded top corners with corner radius $= W_{\rm top/2}$, fin body doping concentration $=$ 1e18 1/cm^3.

dependent on both the doping concentration and the fin shape. Selecting the best doping profile for a particular fin shape is critical for trading off these two competing mechanisms to achieve the minimal total leakage.

To evaluate the impact of fin shape on $I_{\rm OFF}$, we sweep $W_{\rm top}$ over the range of 1–15 nm (Fig. 6, upper left panel). We simulate both the rectangular and triangular optimal doping profiles. $I_{\rm OFF}$ decreases as $W_{\rm top}$ decreases except for the nFinFET with 1e18 1/cm^3 fin body doping when $W_{\rm top}$ is less than 5 nm. The leakage current is more sensitive to $W_{\rm top}$ with the lower doping profile. To obtain the optimal leakage performance for various fin shapes, the doping concentration and fin shape must be selected jointly to optimize performance. A doping concentration of 1e18 1/cm^3 is selected when $W_{\rm top}$ is greater than or equal to 5 nm and a doping concentration of 5e17 1/cm^3 is selected when $W_{\rm top}$ is less than 5 nm. For these $W_{\rm top}$ and doping selections, $V_{\rm th}$ is within the range of 407–458 mV, SS is less than 75 mV/dec, and $I_{\rm ON}/I_{\rm OFF}$ monotonically increases as $W_{\rm top}$ decreases. Therefore, varying $W_{\rm top}$ between 1–15 nm produces a multitude of transistor design choices

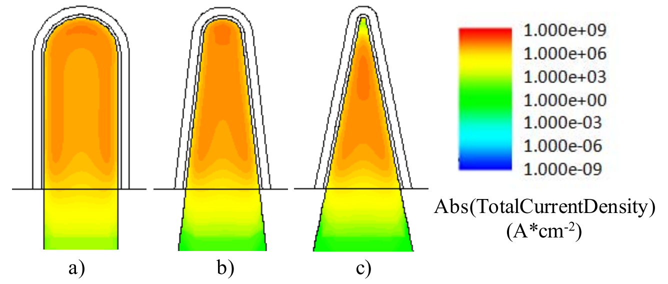

Fig. 8. Ion current density distribution of nFinFET with (a) rectangular fin cross section ($W_{\rm top} = 15$ nm), (b) trapezoidal fin cross section ($W_{\rm top} = 7$ nm), and (c) triangular fin cross section ($W_{\rm top} = 1$ nm), cut at the middle of channel. Rounded top corners with corner radius $= W_{\rm top/2}$, fin body doping concentration $=$ 1e18 1/cm^3.

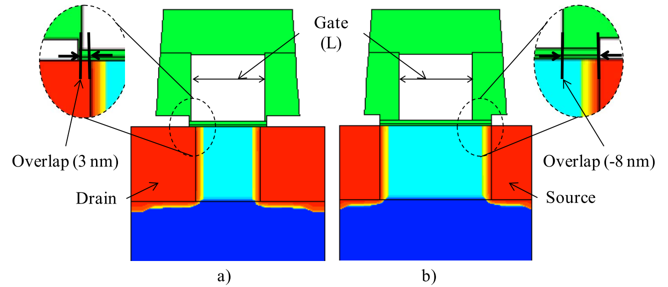

Fig. 9. Cross section of two extreme G–S/D overlap scenarios (a) 3 nm overlap and (b) −8 nm overlap (underlap); cut through the center of fin.

in terms of leakage performance while retaining transistor quality.

Fig. 7 provides insight into the means by which fin shape reduces $I_{\rm OFF}$. As $W_{\rm top}$ decreases, the leakage current is forced into the center of the fin volume. The current density is greatly reduced with the thinner fin.

Reliability is an important consideration for very thin fins. The maximum current density (Fig. 8) for the triangular nFinFET is not in the top narrowest portion of the fin. Instead, the maximum current density distribution is pushed into the fin volume due to quantum confinement. Corner effects have been minimized by maximizing the corner radius for each $W_{\rm top}$. Therefore, we do not expect reliability degradation of the triangular nFinFET due to thermal stress at the narrow fin top.

B. Creating Multithreshold FinFETs via Fin Shape

We observe from Fig. 6 that fin shape provides the ability to trade $I_{\rm ON}$ for $I_{\rm OFF}$, while maintaining good $V_{\rm th}$, SS, and $I_{\rm ON}/I_{\rm OFF}$, making fin shape an excellent candidate for multithreshold nFinFET design. Multithreshold nFinFETs can be constructed by manufacturing different fin shapes within a single IC. For example, a high-drive strength rectangular nFinFET with $W_{\rm top} = 15$ nm has $I_{\rm ON} = 452$ μA/μm, $I_{\rm OFF} = 68.0$ pA/μm, and $V_{\rm th} = 407$ mV, while a low-leakage triangular nFinFET with $W_{\rm top} = 1$ nm has $I_{\rm ON} = 318$ μA/μm, $I_{\rm OFF} = 20.7$ pA/μm, and $V_{\rm th} = 458$ mV. Therefore, a 70% reduction in leakage is achievable at the expense of a 30% reduction in drive current.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE II
MULTITHRESHOLD SIMULATION SCENARIOS

Scenario #	Fin Shape W_{top} (nm)	WF Engineering WF (eV)	G-S/D Overlap Overlap (nm)
0	X	X	-8
1	1	X	-7
2	3	X	-6
3	5	X	-5
4	7	5.0	-4
5	9	4.9	-3
6	11	4.8	-2
7	13	4.7	-1
8	***15***	***4.6***	***0***
9	X	4.5	1
10	X	X	2
11	X	X	3

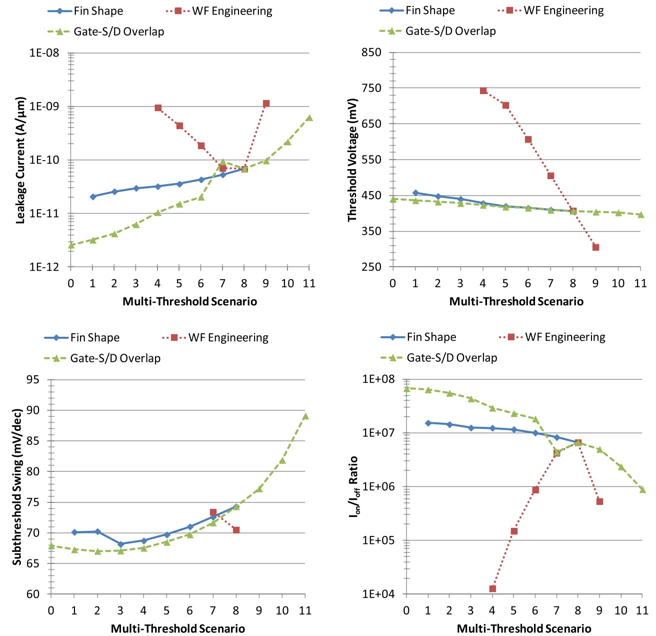

Fig. 10. Multithreshold comparison of WF engineering, G–S/D overlap, and fin shape: I_{OFF} (top left), V_{th} (top right), SS (bottom left), $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio (bottom right).

We further evaluate the merits of using fin shape for multithreshold nFinFET design by comparing with two other multithreshold design techniques: WF engineering and G–S/D overlap. Because we optimize the doping profile to minimize leakage, we do not evaluate doping-controlled multithreshold nFinFETs proposed in [5]. WF is controlled directly as a parameter in the simulation. The G–S/D overlap requires modifying the source/drain implants, and for negative values of overlap (underlap), extending the gate dielectric and spacers as shown in Fig. 9. All other parameters, including the fixed gate length, are identical to the proposed nFinFET in Section III-A.

We simulate WF over the range 4.5–5.0 eV as reported in [13] and G–S/D overlap over the range −8–3 nm as reported in [3]. These parameters, along with our previously defined range of fin shapes, are collected in several simulation scenarios (Table II). Each multithreshold technique is simulated independent of the other two. The column labeled fin shape represents eight simulation scenarios with W_{top} ranging from 1–15 nm in increments of 2 nm, with the WF set to 4.6 eV and the G–S/D overlap set to zero. The column labeled WF engineering represents six additional simulation scenarios with decreasing values of WF, with $W_{\mathrm{top}} = 15$ nm and zero G–S/D overlap. The column labeled G–S/D overlap represents 12 simulation scenarios, with $W_{\mathrm{top}} = 15$ nm and WF set to 4.6 eV. Scenario 8 is the baseline design with a rectangular fin, zero G–S/D overlap, and a WF of 4.6 eV. Because the ranges for W_{top} and WF require fewer than 12 unique parameter values, we use an X to indicate that no experiment was performed for that technique/scenario pair.

The results of the multithreshold simulations are shown in Fig. 10. While WF engineering (scenarios 4–9) provides over 430 mV of V_{th} control, this technique is not suitable for low-leakage bulk nFinFETs. When WF = 4.5 eV (scenario 9), the gate control over the channel is reduced, increasing I_{OFF} by an order of magnitude over the baseline scenario 8. When the WF is greater than 4.6 eV (scenarios 4–7), GIDL increases for low V_g. This is the result of increasing the gate WF without doping the active fin. The resulting GIDL, measured as the substrate current at the ground-tied body contact, is shown in Fig. 11. The only viable range of WF for low-leakage design is 4.6–4.7 eV (scenarios 7 and 8), and all WF values deviating from the optimized 4.6 eV result in increased leakage and reduced $I_{\mathrm{ON}}/\mathrm{I}_{\mathrm{OFF}}$.

Increasing the G–S/D overlap (scenarios 9–11) results in increased I_{OFF}, while decreasing the G–S/D overlap (scenarios 7 to 0) results in substantially reduced leakage (Fig. 10). $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ improves as the G–S/D overlap decreases (scenarios 11 to 0). The positive G–S/D overlap of 3 nm (scenario 11) results in $I_{\mathrm{ON}} = 555$ μA/μm and $I_{\mathrm{OFF}} = 624.5$ pA/μm. The negative G–S/D overlap of −8 nm (scenario 0) results in $I_{\mathrm{ON}} = 174$ μA/μm and $I_{\mathrm{OFF}} = 2.6$ pA/μm. This technique enables a 99.6% reduction in leakage at the expense of a 69% reduction in saturation current. The overlap of −1 nm in scenario 7 is an outlier for the I_{OFF} and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ trends; this is due to GIDL caused by the residual drain implant doping in the channel under the corner of the gate.

The G–S/D overlap range provides 44 mV of V_{th} control. The SS improves with decreasing G–S/D overlap until the overlap exceeds 6 nm, with a total range of 22.1 mV/dec. The SS of 89.1 mV/dec, potentially leading to slower transitions, must be considered against the benefit of increased drive strength. While the G–S/D overlap is extremely effective in controlling leakage, extending the source and drain away from the channel may require increasing the length of the transistor, consuming an additional IC area.

Reducing the top fin width (scenarios 8 to 1) enables a 70% reduction in I_{OFF} and improved $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ (Fig. 10). This technique provides 51 mV of V_{th} control. The jump in SS for scenarios 1 and 2 is due to the change in fin body doping profile.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

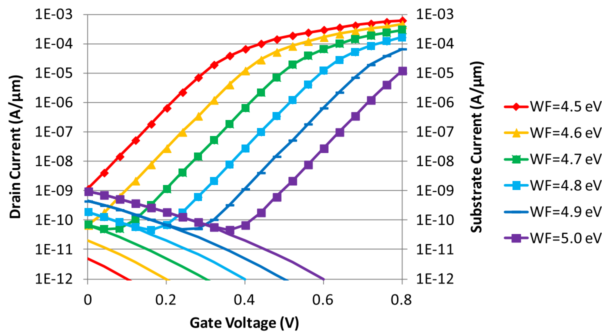

Fig. 11. Drain and substrate current as a function of gate bias, $V_d = 0.8$ V. When the WF is greater than 4.6 eV, the GIDL (measured at the substrate contact) dominates the nFinFET leakage performance. The lines with markers are associated with the left axis and lines without markers are associated with the right axis.

The total range of SS is 6.1 mV/dec. The improvement in I_{OFF} is substantial with minimal impact on V_{th}, SS, and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$. Fin shape provides less total leakage control than G–S/D overlap. However, reducing W_{top} results in a thinner fin and consumes no additional IC area. Also, because the nFinFET footprint is not affected, there is no impact on chip layout.

Our proposed technique for producing multithreshold FinFET devices introduces manufacturing challenges. Fabricating devices with various sidewall angles requires implementing additional processing steps and etch chemistries. While current manufacturing processes have not yet implemented such capabilities, orientation selective etch techniques have been demonstrated to control the fin sidewall angle independent of the fin width [10]. To achieve two different fin shapes, it may be necessary to form each shape separately, duplicating several process steps. Further, it may be necessary to keep each fin type in separate regions of the die to protect one set of fins while processing the other.

An additional challenge is assessing the impact of process variability on FinFET performance. While designing an intrinsic active fin minimizes the impact of random dopant fluctuations, other variation sources must be considered. The fin line-edge-roughness, which is closely related to the techniques used to control fin cross section, has a major impact on the rectangular FinFET performance [21]. Metal gate granularity, which has a strong dependence on the grain size and its orientation, has been shown to impact SOI FinFETs [22] and planar devices [23]. The statistical variability of these factors along with more traditional factors, such as gate length, fin width, and oxide thickness, must be evaluated over different fin shapes.

C. Ultralow Leakage FinFETs

For ultralow power applications, is it desirable to design devices with the lowest possible leakage. From the data in the prior section we observe that the fin shape and G–S/D overlap techniques can be utilized together to generate ultralow leakage FinFETs. We simulated a triangular nFinFET with G–S/D overlap of −8 nm. This device results in a 99% reduction in I_{OFF} over the baseline scenario 8 (I_{OFF} = 0.66 pA/μm), with I_{ON} = 88.6 μA/μm, V_{th} = 506 mV, SS= 67.7 mV/dec and $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 1.34\mathrm{e}8$.

To put our results in perspective, the low power logic from Intel on which our design is based [15] achieves $I_{\mathrm{ON}} = 410$ μA/μm and $I_{\mathrm{OFF}} = 30$ pA/μm with $L = 34$ nm and $V_{\mathrm{dd}} = 0.75$ V. Our triangular nFinFET with $L = 34$ nm and $V_{\mathrm{dd}} = 0.8$ V achieves a 31% reduction in leakage at the expense of 22% less saturation current. Combining our triangular nFinFET with a −8 nm G–S/D overlap results in two orders of magnitude leakage reduction for a 78% reduction in saturation current.

IV. Conclusion

We evaluated the impact of fin cross-section shape on bulk tri-gate nFinFETs with thin fins. We have shown that fin shape has considerable impact on leakage performance. With appropriate doping optimization, a 22-nm nFinFET with triangular fin cross section results in a 70% reduction in leakage current over a rectangular fin with the same base fin width.

We also explored the application of fin shape to multithreshold nFinFET design. Controlling the fin shape provides an effective, area-efficient method to achieve multithreshold design. Rectangular nFinFETs result in $I_{\mathrm{ON}} = 452$ μA/μm, $I_{\mathrm{OFF}} = 68.0$ pA/μm, and $V_{\mathrm{th}} = 407$ mV, while low-leakage triangular nFinFETs result in $I_{\mathrm{ON}} = 318$ μA/μm, $I_{\mathrm{OFF}} = 20.7$ pA/μm, and $V_{\mathrm{th}} = 458$ mV. Our shape-controlled multithreshold nFinFET technique provides chip designers the ability to control the leakage/saturation current tradeoff without consuming any additional IC real estate or impacting chip layout. However, future research is needed to improve the range of threshold and leakage control for multithreshold bulk FinFETs.

We have shown that multithreshold techniques based on WF engineering are not appropriate for bulk FinFET processes with undoped active fins. Finally, our multithreshold technique is compatible with a previously reported G–S/D overlap multithreshold technique, together enabling nFinFETs with less than 1 pA/μm standby current for ultralow-power applications.

References

[1] S. Damaraju *et al.*, "A 22 nm IA multi-CPU and GPU system-on-chip," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 55. Feb. 2012, pp. 56–57.

[2] C. Auth *et al.*, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. IEEE Symp. Very Large Scale Integr. Syst. (VLSI) Technol.*, Jun. 2012, pp. 131–132.

[3] S. A. Tawfik and V. Kursun, "Multi-threshold voltage FinFET sequential circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 1, pp. 151–156, Jan. 2011.

[4] B. J. Sheu *et al.*, "Enabling circuit design using FinFETs through close ecosystem collaboration," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, Jun. 2013, pp. T110–T111.

[5] C.-H. Lin *et al.*, "Channel doping impact on FinFETs for 22 nm and beyond," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, Jun. 2012, pp. 15-16.

[6] C. R. Manoj, M. Nagpal, D. Varghese, and V. R. Rao, "Device design and optimization considerations for bulk FinFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 609–615, Feb. 2008.

[7] N. Collaert *et al.*, "Multi-gate devices for the 32 nm technology node and beyond," *Solid-State Electron.*, vol. 52, no. 9, pp. 1291–1296, 2008.

[8] ITRS. (2011). *Front End Processes (FEP)* [Online] Available: http://www.itrs.net/Links/2011ITRS/2011Chapters/2011FEP.pdf

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[9] Y.-K. Choi, D. Ha, T.-J. King, and J. Bokor, "Investigation of gate-induced drain leakage (GIDL) current in thin body devices: Single-gate ultra-thin body, symmetrical double-gate, and asymmetrical double-gate MOSFETs," *Jpn. J. Appl. Phys.*, vol. 42, no. 4B, pp. 2073–2076, 2003.

[10] Y. Liu *et al.*, "Cross-sectional channel shape dependence of short-channel effects in fin-type double-gate metal oxide semiconductor field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 43, no. 4B, pp. 2151–2155, 2004.

[11] K. Wu, W.-W. Ding, and M.-H. Chiang, "Performance advantage and energy saving of triangular-shaped FinFETs," in *Proc. Int. Conf. Simul. Semicond. Process. Devices (SISPAD)*, Sep. 2013, pp. 143–146.

[12] K.-R. Han, B.-K. Choi, H.-I. Kwon, and J.-H. Lee, "Design of bulk fin-type field-effect transistor considering gate work-function," *Jpn. J. Appl. Phys.*, vol. 47, no. 6R, pp. 4385–4391, 2008.

[13] S. A. Tawfik and V. Kursun, "Work-function engineering for reduced power and higher integration density: An alternative to sizing for stability in FinFET memory circuits," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2008, pp. 788–791.

[14] *Three-Dimensional Simulation of 20 nm FinFETs with Round Fin Corners and Tapered Fin Shape*, TCAD Sentaurus, Synopsys Inc., Mountain View, CA, USA, 2012.

[15] C.-H. Jan *et al.*, "A 22nm SoC platform technology featuring 3-D tri-gate and high-*k*/metal gate, optimized for ultra low power, high performance and high density SoC applications," in *IEDM Tech. Dig (IEDM) Tech. Dig.*, Dec. 2012, pp. 3.1.1–3.1.4.

[16] J. D. Bude, "MOSFET modeling into the ballistic regime," in *Proc. Int. Conf. Simul. Semicond. Process. Devices*, 2000, pp. 23–26.

[17] *Advanced Calibration for Device Simulation User Guide*, Synopsys Inc., Mountain View, CA, USA, 2012.

[18] (2011). *Three-Dimensional Simulation of 16 nm FinFETs with Line Edge Roughness*, TCAD Sentauras, Synopsys Inc., Mountain View, CA, USA [Online]. Available: http://solvnet.synopsys.com/retrieve/033823.html

[19] *Sentaurus Device Monte Carlo User Guide*, Synopsys Inc., Mountain View, CA, USA, 2012.

[20] A. Schenk, "Rigorous theory and simplified model of the band-to-band tunneling in silicon," *Solid-State Electron.*, vol. 36, no. 1, pp. 19–34, 1993.

[21] E. Baravelli, A. Dixit, R. Rooyackers, M. Jurczak, N. Speciale, and K. de Meyer, "Impact of line-edge roughness on FinFET matching performance," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2466–2474, Sep. 2007.

[22] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 5.4.1–5.4.4.

[23] A. R. Brown, N. M. Idris, J. R. Watling, and A. Asenov, "Impact of metal gate granularity on threshold voltage variability: A full-scale three-dimensional statistical simulation study," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1199–1201, Nov. 2010.

Brad D. Gaynor received the B.S., M.S., and Ph.D. degrees in computer and electrical engineering from Tufts University, Medford, MA, USA, in 2001, 2002, and 2014, respectively.

He is currently a Program Manager with Draper Laboratory, Cambridge, MA, USA, where he runs the Cyber Systems business.

Soha Hassoun (SM'07) received the B.S.E.E. degree from South Dakota State University, Brookings, SD, USA, in 1986, the master's degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1988, and the Ph.D. degree from the Department of Computer Science and Engineering, University of Washington, Seattle, WA, USA, in 1997.

She is currently the Chair of the Department of Computer Science at Tufts University, Medford, MA, USA.